# 2022

# COMPUTER SCIENCE

## [HONOURS]

## (CBCS)

## (B.Sc. First Semester End Examination-2022)

## PAPER-CC2T

## [Computer System Architecture]

***Full Marks: 40*** ***Time: 02 Hrs***

*The figures in the right hand margin indicate marks*

*Candidates are required to give their answers in their own words as far as practicable*

*Illustrate the answers wherever necessary*

## Group-A

**1. Answer any five questions of the following: 5x2=10**

a) Show the realization of two-input OR gate using NAND gates only.

b) Consider the statement "$a \oplus b \oplus c = \bar{a} \odot b \odot \bar{c}$". Do yopu think this statement is correct? Justify in brief.

c) Find the binary equivalent of decimal number -14 in 2's complement representation in 8-bit register.

d) What is write through cache?

e) Suppose, a CPU has word size 8-bit and is connected with a memory of size 4 KB. What will be the minimum length of

memory data register and memory address register for this system?

f) Suppose a program P consists of 150 instructions. The clock cycles consumed by each of these instructions is 5. What will be the total execution time for a 4 MHz CPU to execute this program P

g) Suppose, a computer architecture has 8-bit opcode format. Maximum how many instructions can be encoded in this opcode format?

h) Performsubtraction by 2's complement method: 100 -110000.

## Group-B

**Answer any four questions of the following:** **4x5 = 20**

2. Realize the Boolean function using a 8x1 multiplexer:

$f(x,y,z) = \sum(m_0, m_2, m_4, m_6, m_7)$ 5

3. Write a short note on microproammed control unit with a suitable diagram. 5

4. What is race condition in flipflop? Show how can we obtain a T flip from a J-K flip flop. 2+3

5. Prove that in ideal case, maximum speedup achievable by a k-stage instruction pipeline processor would be k.

6. a) Simplify the following Boolean function using Karnaugh map:

$f(a,b,c,d) = \sum(m_1, m_2, m_3, m_7, m_8, m_{12}, m_{14})$



b) Perform the subtraction 110-1010 using 2's complement representation. 3+2

7. a) Design a 3-bit left-shift register using J-K flip-flops.

b) Realize EX-OR gate using NAND gates only.

## Group –C

**Answer any one question:** **1x10 = 10**

8. a) A CPU employs 5-stage instruction pipeline execution. Time taken by opcode fetch, instruction decode, read operand, execute operation and write result stages are 5ms, 2ms, 4ms, 2ms, and 4ms respectively. A program P consists of 250 instructions all of which are non-brunching instructions. Calculate the total execution time of P 4

b) What do you mean by cycle stealing mode of DMA operation? What is polling method of resolving the priority of interrupting devices? 3+3

9. a) Explain Booth's multiplication algorithm.

b) Perform -5x4 using this algorithm. 5+5

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