2021

Computer Science

[P.G.]

(CBCS)

(M.Sc. First Semester End Examination-2021)

PAPER- CS-102

(Computer Organization Architecture)

Full Marks: 40 ***Time: 02 Hrs***

The figures in the right hand margin indicate marks

Candidates are required to give their answers in their own words as far as practicable

Illustrate the answers wherever necessary

Group A

1. Answer any FIVEquestions of the following: 5x2=10

a) State Andahl's laws.

b) Justify the statement: K-stage pipeline can have maximum speed up K.

c) How many distinct Boolean functions are there with three Boolean variables?

d) What is direct-mapped cache?

e) How does micro / programmed control unit differ from hardwired control unit?

f) What is vector instruction format?

g) Compare among temporal spatial and sequential locality of memory hierarchy.

h) What is structural hazard?

Group B

Answer any FOUR questions of the following: 5x4 = 20

2. Implement a Boolean function $f = \sum(1,2,3,5,6,12)$ using a 8x1 MUX.
3. Design a mod-6 asynchronous counter.
4. Suppose, we replace a sequential execution processor by pipelined instruction processor. The pipelined instruction execution has five stages: IF (8ns), ID (4 ns), RD (9ns), EX (2ns) and WR (9ns).The values in paranthesis indicate time taken by these pipeline stages of instruction execution. If no time is wasted to move from one pipeline stage to next pipeline stage, find the speed up achieved to execute a program of 100 instructions over sequential execution.
5. Write a short note on technique to reduce miss penalty of cache memory.
6. a) What is multiple computer system?

   b) Explain UMA model of multiprocessor system with diagram.
7. What is array processor with a block diagram

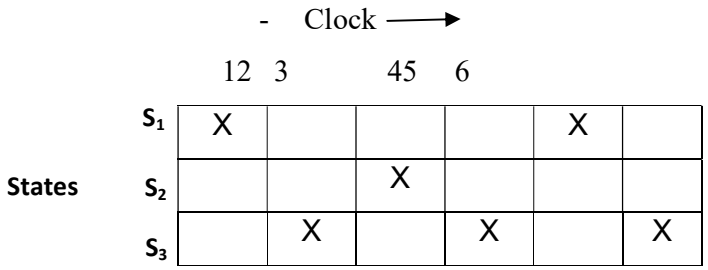
Group C

Answer any ONE questions of the following: 10x1 = 10

8. a) How will the decimal number -18.25 be represented in IEEE-754 32-bit representation in Hexa-decimal form?

   Remember, IEEE-754 standard for 32-bit representation uses 23 least significant bits for mantissa, next 8-bits for exponent, and MSB for sign bit

   b) What is principle of locality in memory?
9. Consider the following reservation table of a pipeline processor-



a) Find all forbidden and non-forbidden latencies.

b) Draw state transition diagram.

c) List all simple and greedy cycles.

d) Calculate minimum overage latency.