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RNLKWC/B.Sc./CBCS/BCA/HIS/C4T/22

2022

BCA

[Honours]

(B.Sc. Second Semester End Examination-2022)

PAPER-C4T

Full Marks: 40

Time: 02 Hrs

The figures in the right hand margin indicate marks

Candidates are required to give their answers in their own words as far as practicable

Illustrate the answers wherever necessary

Group A

1) Answer any Five questions:

2x5 = 10

- a. Write the difference between SRAM and DRAM.
- b. What is an instruction cycle?
- c. Why every computer system is associated with a set of general purpose registers?
- d. How do we know the size of memory through address bus?
- e. What do you mean by direct addressing mode?
- f. State the difference between RISC and CISC.
- g. What do you mean by access time and bandwidth of a memory?
- h. What are the difference between low-level language and high-level language?

(2)

Group B

Answer any Four Questions:

4x5 = 20

2. a) What is the functions of control unit?
b) How does hardwired control unit differ from microprogrammed control unit 2+3
3. What do you mean by computer instructions? Describe Two address instructions and Three-address instructions with example. 1+4
4. a) What is write through cache?
b) Write the characteristics of secondary memory. What do you mean by Direct mapping?
5. Explain DMA mode of data transfer. Where does DMA mode of data transfer find its use?
6. a) Write notes on stack organisation.
b) Differentiate between Machine language and Assembly language 3+2
7. a) Explain the common bus system in computer architecture.
b) Suppose, a CPU has word size 16 bit and is connected with a memory of size 8 KB. Then What will be the minimum length of data register (DR) and address register (AR), for this system? 4+1

Group C

Answer any One Question:

1x10 = 10

8. a) What are the major function of I/O Module?

(3)

- b) What do you mean by addressing modes Explain various addressing modes. 2+8
 9. What is carry look-ahead adder (CLA)? Design a 4-bit CLA. What are its merits and demerits? Estimate the maximum propagation delay for n-bit CLA. 1+5+3+1
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